Remarks

Reconsideration of this Application is respectfully requested.

Applicant respectfully requests admission of the foregoing amendment to place the application in condition for allowance by traversing the rejections under 35 U.S.C. § 103.

Upon entry of the foregoing amendment, claims 1-7, 9-24, 26, 27, 29-32, and 40-43 are pending in the application, with claims 1, 10, and 27 being the independent claims. Claims 17 and 31 are sought to be amended. These changes are believed to introduce no new matter and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Telephonic Interview

Applicant and Applicant's representatives wish to thank Examiner Thomas J. Cleary for the telephonic interview with Applicant's representatives, Mr. David C. Isaacson and Mr. Timothy A. Doyle, on December 5, 2008. During the interview, Applicant's representatives and the Examiner discussed the rejections of the pending claims. The substance of the interview is incorporated in the following remarks.

Rejections Under 35 U.S.C. § 103

MCF5206, Addendum, Watanabe, and Beckert

Paragraph 2 of the Office Action rejected claims 1, 2, 4-7, 9-14, 16, 17, 20-24, and 40-43 under 35 U.S.C. § 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" ("MCF5206"), Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" ("Addendum"), U.S. Patent No. 5,025,368 to Watanabe ("Watanabe"), and U.S. Patent No. 6,499,078 to Beckert *et al.* ("Beckert"). For at

least the following reasons, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

Claim 1 recites, in part, "a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities[.]" Claim 10 recites, in part, "the first interrupts having architecturally fixed interrupt priorities[.]" Applicant respectfully submits none of MCF5206, Addendum, Watanabe, and Beckert, whether taken alone, or in combination, discloses at least these features of claims 1 and 10.

The Examiner, at pages 18 and 19 of the Office Action, states, in part:

> The 5206 User's Manual further discloses that the "*interrupt level*" is an indication of priority, as Level 7 is the highest priority, and Level 1 is the lowest (See Page 7-11), while the "*interrupt priority*" is an identifier (sub-priority) which identifies which interrupt is being acknowledged (See Page 7-6). Thus, the MCF5206 does disclose a mode of operation in which the external interrupts have an architecturally fixed interrupt priority which is represented by the interrupt level. The Examiner further notes that the claim language does not prohibit the external interrupts from having identifiers (sub-priorities) which are programmable. The claims only require that the external interrupts have architecturally fixed interrupt priorities. The interrupt level of the MCF5206 for the external interrupts, which defines the priority of the external interrupt with respect to the other interrupt levels, is architecturally fixed, as evidenced by the 5206 User's Manual (See Page 7-4).

As explained during the Examiner's Interview, Applicant respectfully asserts the MCF5206 does not disclose "architecturally fixed interrupt priorities" as recited in claims 1 and 10.

As recited on page 7-10 of MCF5206, "[e]ach interrupt input must have a unique interrupt level and interrupt priority combination." (Emphasis added.) Additionally, page 7-4 of MCF5206 provides:

> Although the interrupt levels of the external interrupts are fixed, customers can program the interrupt priorities of the external interrupts to any value using the IP (IP1, IP0) bits in the corresponding interrupt control registers (ICR7 - ICR1).

(Emphasis added.) Further, page 7-11 of MCF5206 recites:

> IP[1:0]- Interrupt Priority
> These bits indicate the priority within an interrupt level assigned to each interrupt. You can assign as many as four interrupts to the same interrupt level as long as they have unique interrupt priorities. IP1-IP0 = 3 is the highest priority, and IP1-IP0 = 0 is the lowest priority for a given interrupt level.

(Emphasis added.)

Thus, MCF5206 discloses: (1) each interrupt input must have both an interrupt level and an interrupt priority and (2) the interrupt priority is programmable. Importantly, Applicant can find no disclosure, teaching, or suggestion in MCF5206 of a situation in which both interrupt level and interrupt priority are fixed. It is axiomatic that a priority determinant that has two portions, one of which is programmable, is as a whole programmable. This is precisely the case with the priority determinant disclosed in MCF5206.

During the Examiner's Interview and contrary to the express disclosure in MCF5206 provided above, the Examiner contends that for interrupts directed to the same level, the interrupt priority bits perform an interrupt identification function rather than a priority determining function. To support this position, the Examiner refers to page 7-6 of MCF5206, which provides:

> You can assign as many as four interrupts to the same interrupt level, but you must assign unique interrupt priorities. The interrupt controller uses the interrupt priorities during an interrupt acknowledge cycle to determine which interrupt is being acknowledged. The interrupt priority bits determine the appropriate interrupt being acknowledged when multiple interrupts are assigned to the same level and are pending when the interrupt-acknowledge cycle is generated.

(Emphasis added.)

While Applicant disputes the Examiner's contention, even assuming, *arguendo*, the interrupt priority performs an identification function for interrupts directed to the same level, Applicant respectfully submits there is no disclosure, teaching, or suggestion in MCF5206

that such identification function is in any way divorced from, overrides, or otherwise precludes the primary purpose of the programmable interrupt priorities to determine priorities of interrupt inputs. Indeed, the passage from MCF5206 to which the Examiner refers strongly suggests that when multiple interrupt inputs are directed to the same level during an interrupt acknowledge cycle (i.e., when priority cannot be determined based upon the level), interrupt priorities must determine the priorities of the interrupt inputs. Because the level is the same, the level bits cannot be used to determine priority for interrupts directed to the level. That function, rather, must be the handled by the programmable interrupt priority.

In summary, Applicant respectfully submits that MCF5206 does not disclose, teach, or suggest "architecturally fixed interrupt priorities" as recited in claims 1 and 10. Moreover, Applicant respectfully submits none of Addendum, Watanabe, and Beckert overcomes the deficiency of MCF5206.

Consequently, Applicant respectfully asserts independent claims 1 and 10 are patentable over MCF5206, Addendum, Watanabe, and Beckert. Claims 2, 4-7, 9, 11-14, 16, 17, 20-24, and 40-43, and 38-42 depend from claims 1 or 10 and are therefore also patentable over MCF5206, Addendum, Watanabe, and Beckert. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1, 2, 4-7, 9-14, 16, 17, 20-24, and 40-43, and 38-42 set forth in paragraph 2 of the Office Action.

MCF5206, Addendum, and Watanabe

Paragraph 26 of the Office Action rejected claims 27, 29, and 30 under 35 U.S.C. § 103(a) as being unpatentable over MCF5206, Addendum, and Watanabe. For at least the following reasons, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

Claim 27 recites, in part, "receiving the core generated interrupts, the core generated interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts[.]" As explained above with respect to claims 1 and 10, Applicant respectfully submits that none of MCF5206, Addendum, and Watanabe, whether taken alone or in combination, discloses, teaches, or suggests "architecturally fixed interrupt priorities " as recited in claim 27.

Consequently, Applicant respectfully asserts independent claim 27 is patentable over MCF5206, Addendum, and Watanabe. Claims 29 and 30 depend from claim 27 and are therefore also patentable over MCF5206, Addendum, and Watanabe. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 27, 29, and 30 set forth in paragraph 26 of the Office Action.

MCF5206, Watanabe, Beckert, and Agrawal

Paragraph 30 of the Office Action rejected claims 3 and 15 under 35 U.S.C. § 103(a) as being unpatentable over MCF5206, Watanabe, Beckert, and U.S. Patent No. 5,768,500 to Agrawal *et al.* ("Agrawal"). For at least the following reasons, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

As explained above, Applicant respectfully submits claims 1 and 10 are patentable over MCF5206, Watanabe, and Beckert, whether taken alone or in combination. Applicant respectfully submits Agrawal does not overcome the deficiencies of MCF5206, Watanabe, and Beckert. Claims 3 and 15 depend from claims 1 or 10 and are therefore also patentable over MCF5206, Watanabe, Beckert, and Agrawal. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 3 and 15 set forth in paragraph 30 of the Office Action.

MCF5206, Watanabe, Beckert, and Cutler

Paragraph 33 of the Office Action rejected claims 18 and 19 under 35 U.S.C. § 103(a) as being unpatentable over MCF5206, Watanabe, Beckert, and U.S. Patent No. 5,148,544 to Cutler *et al.* ("Cutler"). For at least the following reasons, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

As explained above, Applicant respectfully submits claim 10 is patentable over MCF5206, Watanabe, and Beckert, whether taken alone or in combination. Applicant respectfully submits Cutler does not overcome the deficiencies of MCF5206, Watanabe, and Beckert. Claims 18 and 19 depend from claim 10 and are therefore also patentable over MCF5206, Watanabe, Beckert, and Cutler. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 18 and 19 set forth in paragraph 33 of the Office Action.

MCF5206, Watanabe, Beckert, and Zimmer

Paragraph 36 of the Office Action rejected claims 25 and 26 under 35 U.S.C. § 103(a) as being unpatentable over MCF5206, Watanabe, Beckert, U.S. Patent No. 5,940,587 to Zimmer ("Zimmer"). Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

As explained above, Applicant respectfully submits that claim 10 is patentable over MCF5206, Watanabe, and Beckert, whether taken alone or in combination. Applicant respectfully submits Zimmer does not overcome the deficiencies of MCF5206, Watanabe, and Beckert.

Claim 26 depends from claim 10 and is therefore also patentable over MCF5206, Watanabe, Beckert, and Zimmer. Accordingly, Applicant respectfully requests that the

Examiner reconsider and withdraw the rejection of claim 26 set forth in paragraph 36 of the Office Action.

MCF5206, Watanabe, and Zimmer

Paragraph 39 of the Office Action rejected claims 31 and 32 under 35 U.S.C. § 103(a) as being unpatentable over MCF5206, Watanabe, and Zimmer. For at least the following reasons, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

As explained above, Applicant respectfully submits claim 27 is patentable over MCF5206 and Watanabe, whether taken alone or in combination. Applicant respectfully submits Zimmer does not overcome the deficiencies of MCF5206 and Watanabe.

Claims 31 and 32 depend from claim 27 and are therefore also patentable over MCF5206, Watanabe, and Zimmer. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 31 and 32 set forth in paragraph 39 of the Office Action.

Propriety of the Finality of the Rejections in the Present Office Action

Applicant disputes the propriety of the finality of the rejections in the present Office Action.

Section 706.07(b) of the Manual of Patent Examining Procedure provides:

> The claims of an application for which a request for continued examination (RCE) has been filed may be finally rejected in the action immediately subsequent to the filing of the RCE . . . where all the claims in the application prior to the entry of the submission under 37 CFR 1.114 (A) are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114, and (B) would have been properly finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to the filing of the RCE under 37 CFR 1.114.

Therefore, to determine whether the finality of the rejection if proper, the claims as amended in the submission accompanying the RCE filed on August 14, 2008, must be

considered as if entered prior to the filing of the RCE. If those claims would not have been properly finally rejected in the next Office Action (i.e., the present Office Action), the finality of the Office Action is not proper. In this case, Applicant respectfully asserts the finality of the Office Action is not proper.

The relevant art of record prior to the filing of the August 14, 2008, RCE is MCF5206, Addendum, Watanabe, Beckert, Agrawal, Cutler, and Zimmer. As explained above, none of these references, whether taken alone or in combination, disclose, teach, or suggest "architecturally fixed interrupt priorities." However, each of the claims presented in the submission accompanying the RCE filed August 14, 2008, recited "architecturally fixed interrupt priorities." Because the relevant art of record neither anticipates nor renders obvious the claims presented in the submission accompanying the RCE filed August 14, 2008, Applicant respectfully asserts the claims presented in the August 14, 2008, submission would not have been properly finally rejected on the grounds and art of record in the next Office Action (i.e., the present Office Action) if they had been entered in the application prior to the filing of the RCE under 37 C.F.R. § 1.114. Thus, Applicant respectfully submits that at least part (B) of the requirement to make the present Office Action final has not been satisfied and the finality of the present Office Action is not proper. Accordingly, Applicant respectfully requests the Examiner reconsider and withdraw the finality of the present Office Action.

Conclusion

All of the stated grounds of rejection have been properly traversed. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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